IN THE SPECIFICATION:

Please amend the paragraph beginning on Page 4, line 1, as follows:

--The controller I/O cell 16, shown in detail in Figure 3, may be a typical high speed I/O with the addition of N number of control bits for pull-up and pull-down control of the driver Impedance. The I/O cell also has three additional control inputs PNDRIVE, NOUPDT and TESTUDT all of which come from the digital controller. A typical driver would pass data from an internal pin "A" and drive the data at the output pin "PAD" with a fixed driver impedance for both pull-up and pull-down. In the disclosed I/O cell, the driver impedance depends on the PFET, schematically represented at 12a in Figure 2, control bits (PVTP[5:0]) and NFET control bits (PVTN[5:0]). The input "PNDRIVE" enables a default maximum value of driver impedance to be maintained. When all the control bit inputs are disabled, the output impedance will be at its maximum impedance level when PNDRIVE is enabled. When the controller enables additional input bits PVTP[5:0] and PVTN[5:0], the driver will switch on additional PFET and NFET fingers which will lower the output impedance and increase the drivers current strength. The control bits are binary weighted with bit "0" being the LSB and bit "5" being the MSB. This yields 32 bits of resolution for both the pull-up and pull-down impedance.--

Please amend the paragraph beginning on Page 6, line 12, as follows:

--When the digital controller senses the ZPCNTDWN signal is toggling between one and zero each count, a fixed count PVTP[5:0] is sent to the I/Os and calibration cell. The stable count PVTP[5:0] at the calibration cell is used to control a mirror copy of the PFETs controlled by CNTP[5:0]. This mirror copy of the PFETs is schematically represented at 14a in Figure 2. The impedance of the PFETs controlled by PVTP[5:0] are equal to the external resistor and is used to calibrate the pull down NFET impedance. With a stable count at PVTP[5:0] the digital controller starts to increment the count at CNTN[5:0]. If CNTN[5:0] starts out at 000000, the pull-down NFETs are off and the voltage at VNEVAL is pulled to Vddq through the PFETs controlled by PVTP[5:0]. The output ZNCNTDWN = 0 is sent to the digital controller which forces the binary count at CNTN[5:0] to increment. CNTN[5:0] increases until the voltage at VNEVAL is greater than or equal to the internal reference Vddq/2.--